National Semiconductor

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LPV511
Micropower, Rail-to-Rail Input and Output Operational Amplifier

General Description

The LPV511 is a micropower operational amplifier that operates from a voltage supply range as wide as 2.7V to 12V with guaranteed specifications at 3V, 5V and 12V. The LPV511 exhibits an excellent speed to power ratio, drawing only 880 nA of supply current with a bandwidth of 27 kHz. These specifications make the LPV511 an ideal choice for battery powered systems that require long life through low supply current, such as instrumentation, sensor conditioning and battery current monitoring.

The LPV511 has an input range that includes both supply rails for ground and high side battery sensing applications. The LPV511 output swings within 100 mV of either rail to maximize the signal's dynamic range in low supply applications. In addition, the output is capable of sourcing 650 µA of current when powered by a 12V battery.

The LPV511 is fabricated on National's advanced VIP50C process.

The LPV511 is available in the space saving SC70 package which makes it ideal for portable electronics with area constrained PC boards.

Features

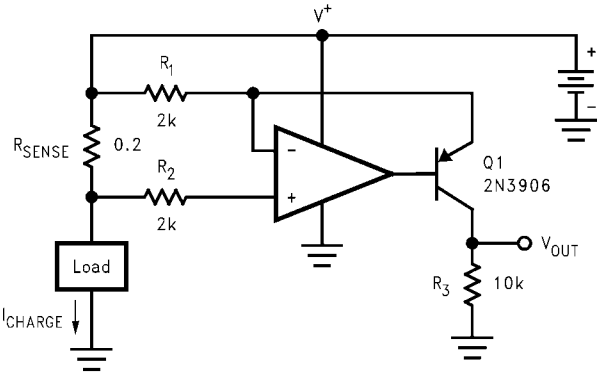
(Typical at 3V supply unless otherwise noted)

- Wide supply voltage range 2.7V to 12V
- Slew rate 7.7 V/ms
- Supply current 880 nA
- Output short circuit current 1.35 mA
- Rail-to-rail input
- Rail-to-rail output 100 mV from rails
- Bandwidth (C_L = 50 pF, R_L = 1 MΩ) 27 kHz
- Unity gain stable

Applications

- Battery powered systems
- Security systems
- Micropower thermostats
- Solar powered systems
- Portable instrumentation
- Micropower filter
- Remote sensor amplifier

Typical Application



$$V_{OUT} = \frac{R_{SENSE} \bullet R_3}{R_1} \bullet I_{Charge} = 1\Omega \bullet I_{Charge}$$

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High Side Battery Current Sensor

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	
Human Body	2 KV
Machine Model	200V
V_{IN} Differential	2.1V
Supply Voltage (V^+ - V^-)	13.2V
Voltage at Input/Output pins	V^+ +0.3V, V^- −0.3V
Storage Temperature Range	−65°C to +150°C
Short Circuit Duration	(Note 4)
Junction Temperature (Note 3)	+150°C
Soldering Information	
Infrared or Convection (20 sec)	235°C
Wave Soldering Lead Temp. (10 sec)	260°C

Operating Ratings (Note 1)

Temperature Range (Note 3)	−40°C to +85°C
Supply Voltage ($V^+ - V^-$)	2.7V to 12V
Package Thermal Resistance (θ_{JA} (Note 3))	
5-Pin SC70	456°C/W

3V Electrical Characteristics (Note 5)

Unless otherwise specified, all limits are guaranteed for T_J = 25°C, V^+ = 3V, V^- = 0V, $V_{CM} = V_O = V^+/2$, and R_L = 100 kΩ to $V^+/2$. **Boldface limits apply to the temperature range of −40°C to 85°C.**

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 7)	Max (Note 6)	Units
V_{OS}	Input Offset Voltage			±0.2	±3 **±3.8**	mV
TC V_{OS}	Input Offset Voltage Drift	(Note 8)		±0.3	**±15**	µV/°C
I_B	Input Bias Current (Note 9)	V_{CM} = 0.5V	−1000 **−1600**	−320		pA
		V_{CM} = 2.5V		110	800 **1900**	
I_{OS}	Input Offset Current			±10		pA
CMRR	Common Mode Rejection Ratio	V_{CM} Stepped from 0V to 1.5V	77 **70**	100		dB
		V_{CM} Stepped from 2.4V to 3V	75 **68**	115		
		V_{CM} Stepped from 0.5V to 2.5V	60 **56**	80		
PSRR	Power Supply Rejection Ratio	V^+ = 2.7V to 5V, V_{CM} = 0.5V	72 **68**	114		dB
		V^+ = 3V to 5V, V_{CM} = 0.5V	76 **72**	115		
		V^+ = 5V to 12V, V_{CM} = 0.5V	84 **80**	117		
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 50 dB	−0.1 **0**		3.1 **3.0**	V
A_{VOL}	Large Signal Voltage Gain	Sinking, V_O = 2.5V	75 **70**	105		dB
		Sourcing, V_O = 0.5V				
V_O	Output Swing High	V_{ID} = 100 mV	2.85 **2.8**	2.90		V
	Output Swing Low	V_{ID} = −100 mV		100	150 **200**	mV
I_{SC}	Output Short Circuit Current (Note 10)	Sourcing V_{ID} = 100 mV		−500	−225	µA
		Sinking V_{ID} = −100 mV	225	1350		
I_S	Supply Current			0.88	1.2 **1.5**	µA
SR	Slew Rate (Note 11)	A_V = +1, V_O ramps from 0.5V to 2.5V	5.25 **3.10**	7.7		V/ms

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 7)	Max (Note 6)	Units
GBW	Gain Bandwidth Product	R_L = 1 MΩ, C_L= 50 pF		27		kHz
	Phase Margin	R_L = 1 MΩ, C_L= 50 pF		53		deg
e_n	Input-Referred Voltage Noise	f = 100 Hz		320		nV/√Hz
i_n	Input-Referred Current Noise	f = 10 Hz		.02		pA/√Hz
		f = 1 kHz		.01		

5V Electrical Characteristics (Note 5)

Unless otherwise specified, all limits are guaranteed for T_J = 25°C, V+ = 5V, V− = 0V, V_{CM} = V_O = V+/2, and R_L = 100 kΩ to V+/2. **Boldface limits apply to the temperature range of −40°C to 85°C.**

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 7)	Max (Note 6)	Units
V_{OS}	Input Offset Voltage			±0.2	±3 **±3.8**	mV
TC V_{OS}	Input Offset Voltage Drift	(Note 8)		±0.3	**±15**	µV/°C
I_B	Input Bias Current (Note 9)	V_{CM} = 0.5V	−1000 **−1600**	−320		pA
		V_{CM} = 4.5V		110	800 **1900**	
I_{OS}	Input Offset Current			±10		pA
CMRR	Common Mode Rejection Ratio	V_{CM} Stepped from 0V to 2.5V	80 **73**	115		dB
		V_{CM} Stepped from 4.4 to 5V	75 **68**	107		
		V_{CM} Stepped from 0.5 to 4.5V	65 **62**	87		
PSRR	Power Supply Rejection Ratio	V+ = 2.7V to 5V, V_{CM} = 0.5V	72 **68**	114		dB
		V+ = 3V to 5V, V_{CM} = 0.5V	76 **72**	115		
		V+ = 5V to 12V, V_{CM} = 0.5V	84 **80**	117		
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 50 dB	−0.1 **0**		5.1 **5**	V
A_{VOL}	Large Signal Voltage Gain	Sinking, V_O = 4.5V	78 **73**	110		dB
		Sourcing, V_O = 0.5V				
V_O	Output Swing High	V_{ID} = 100 mV	4.8 **4.75**	4.89		V
	Output Swing Low	V_{ID} = −100 mV		110	200 **250**	mV
I_{SC}	Output Short Circuit Current (Note 10)	Sourcing to V− V_{ID} = 100 mV		−550	−225	µA
		Sinking to V+ V_{ID} = −100 mV	225	1350		
I_S	Supply Current			0.97	1.2 **1.5**	µA
SR	Slew Rate (Note 11)	A_V = +1, V_O ramps from 0.5V to 4.5V	5.25 **3.10**	7.5		V/ms
GBW	Gain Bandwidth Product	R_L = 1 MΩ, C_L= 50 pF		27		kHz
	Phase Margin	R_L = 1 MΩ, C_L= 50 pF		53		deg
e_n	Input-Referred Voltage Noise	f = 100 Hz		320		nV/√Hz

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 7)	Max (Note 6)	Units
i_n	Input-Referred Current Noise	f = 10 Hz		.02		pA/$\sqrt{Hz}$
		f = 1 kHz		.01		

12V Electrical Characteristics (Note 5)

Unless otherwise specified, all limits are guaranteed for T_J = 25°C, V^+ = 12V, V^- = 0V, $V_{CM} = V_O = V^+/2$, and R_L = 100 kΩ to $V^+/2$. **Boldface limits apply to the temperature range of −40°C to 85°C.**

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 7)	Max (Note 6)	Units
V_{OS}	Input Offset Voltage			±0.2	±3 **±3.8**	mV
TC V_{OS}	Input Offset Voltage Drift	(Note 8)		±0.3	**±15**	µV/°C
I_B	Input Bias Current (Note 9)	V_{CM} = 0.5V	−1000 **−1600**	−320		pA
		V_{CM} = 11.5V		110	800 **1900**	
I_{OS}	Input Offset Current			±10		pA
CMRR	Common Mode Rejection Ratio	V_{CM} Stepped from 0V to +6V	75 **70**	115		dB
		V_{CM} Stepped from 11.4V to 12V	75 **68**	110		
		V_{CM} Stepped from 0.5V to 11.5	70 **65**	97		
PSRR	Power Supply Rejection Ratio	V^+ = 2.7V to 5V, V_{CM} = 0.5V	72 **68**	114		dB
		V^+ = 3V to 5V, V_{CM} = 0.5V	76 **72**	115		
		V^+ = 5V to 12V, V_{CM} = 0.5V	84 **80**	117		
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 50 dB	−0.1 **0**		12.1 **12**	V
A_{VOL}	Large Signal Voltage Gain	Sinking, V_O = 0.5V	89 **84**	110		dB
		Sourcing, V_O = 11.5V				
V_O	Output Swing High	V_{ID} = 100 mV	11.8 **11.72**	11.85		V
	Output Swing Low	V_{ID} = −100 mV		150	200 **280**	mV
I_{SC}	Output Short Circuit Current (Note 10)	Sourcing V_{ID} = 100 mV		−650	−200	µA
		Sinking V_{ID} = −100 mV	200	1300		
I_S	Supply Current			1.2	1.75 **2.5**	µA
SR	Slew Rate (Note 11)	A_V = +1, V_O ramped from 1V to 11V	5.25 **3.10**	7.0		V/ms
GBW	Gain Bandwidth Product	R_L = 1 MΩ, C_L= 50 pF		25		kHz
	Phase Margin	R_L = 1 MΩ, C_L= 50 pF		52		deg
e_n	Input-Referred Voltage Noise	f = 100 Hz		320		nV/$\sqrt{Hz}$
i_n	Input-Referred Current Noise	f = 10 Hz		.02		pA/$\sqrt{Hz}$
		f = 1 kHz		.01		

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics Tables.

Note 2: Human Body Model: 1.5 kΩ in series with 100 pF. Machine Model: 0Ω in series with 200 pF.

Note 3: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Note 4: Output short circuit duration is infinite for $V^+ < 6V$ at room temperature and below. For $V^+ > 6V$, allowable short circuit duration is 1.5 ms.

Note 5: Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device.

Note 6: Limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlations using the Statistical Quality Control (SQC) method.

Note 7: Typical values represent the most likely parametric norm at the time of characterization.

Note 8: Offset voltage drift is guaranteed by design and/or characterization and is not tested in production. Offset voltage drift is determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.

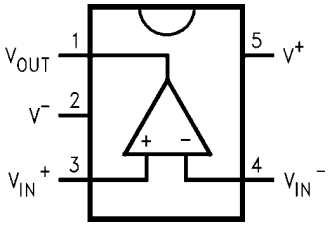
Note 9: Positive current corresponds to current flowing into the device.

Note 10: The Short Circuit Test is a momentary test. See (Note 4).

Note 11: Slew rate is the average of the rising and falling slew rates.

Connection Diagram

SC70-5



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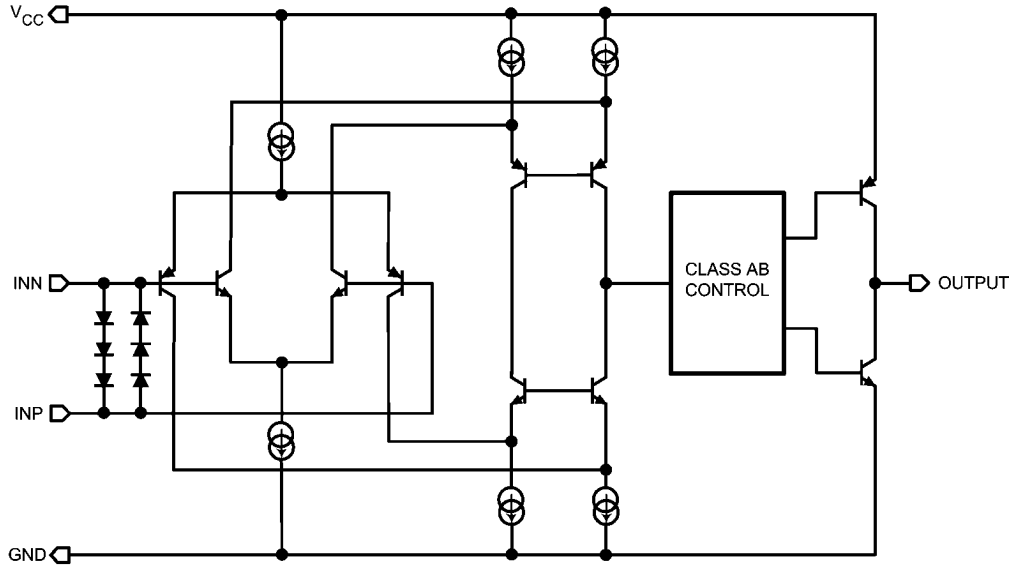
Top View

Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
5-Pin SC70	LPV511MG	A91	1k Units Tape and Reel	MA005A
	LPV511MGX		3k Units Tape and Reel	

Simplified Schematic



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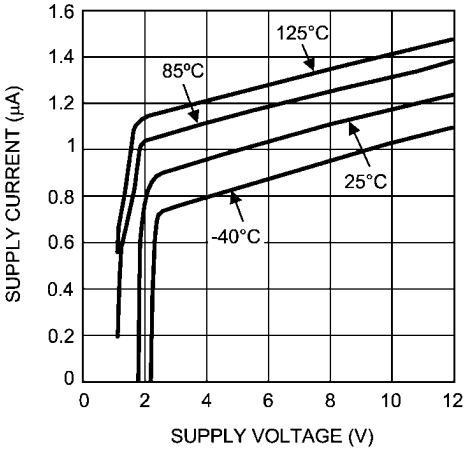
Typical Performance Characteristics

At T_J = 25°C, unless otherwise specified.

Supply Current vs. Supply Voltage



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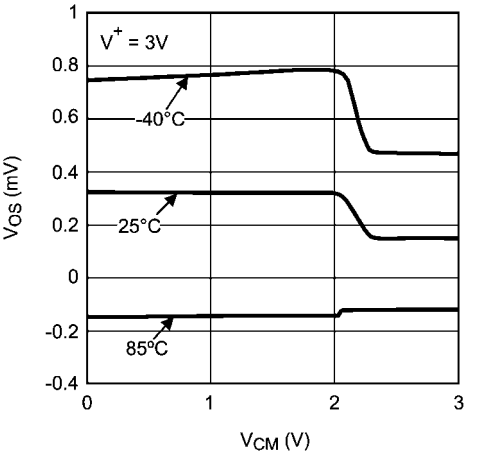
Input Offset Voltage vs. Input Common Mode



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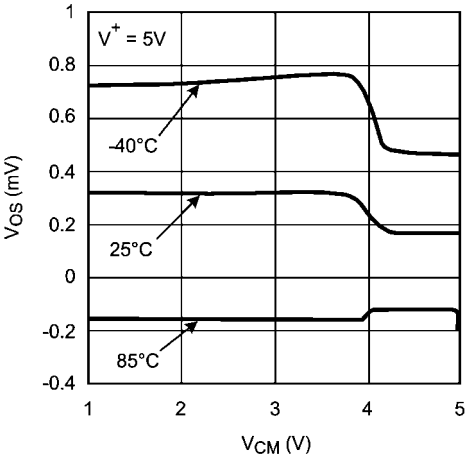
Input Offset Voltage vs. Input Common Mode



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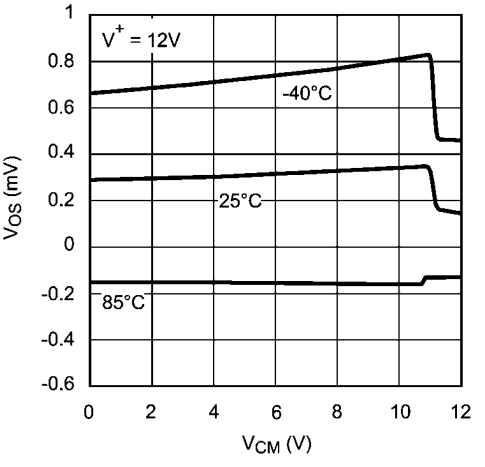
Input Offset Voltage vs. Input Common Mode



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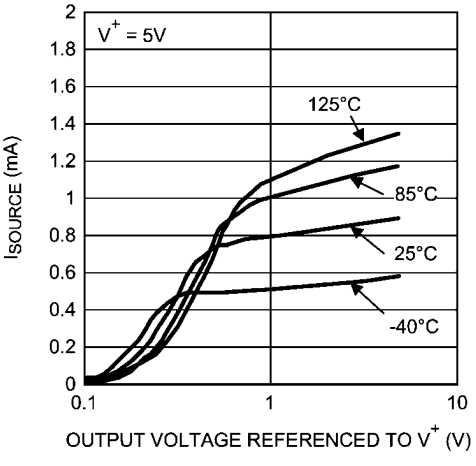
Sourcing Current vs. Output Voltage



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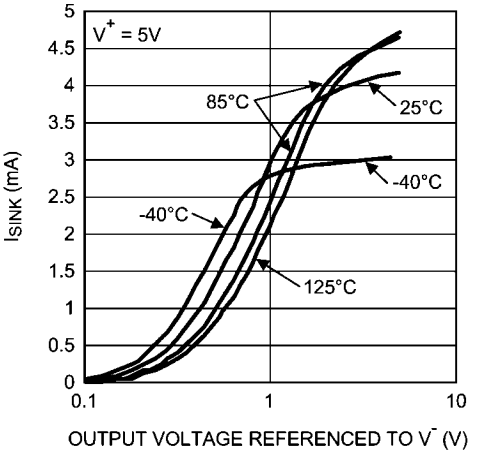
Sinking Current vs. Output Voltage



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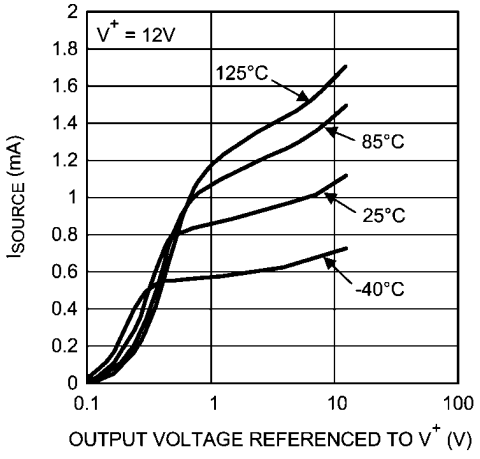
Sourcing Current vs. Output Voltage



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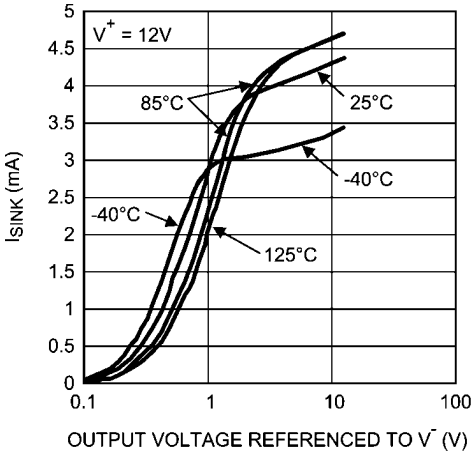
Sinking Current vs. Output Voltage



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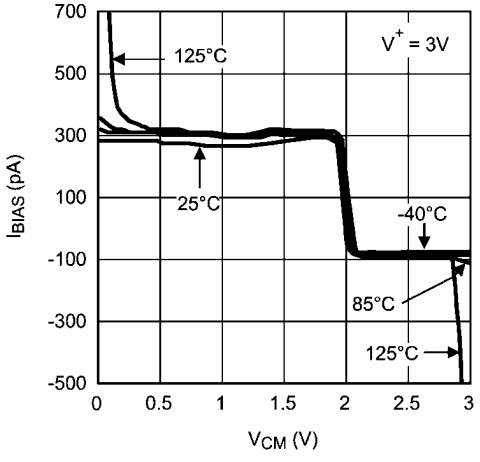
Input Bias Current vs. Common Mode Voltage



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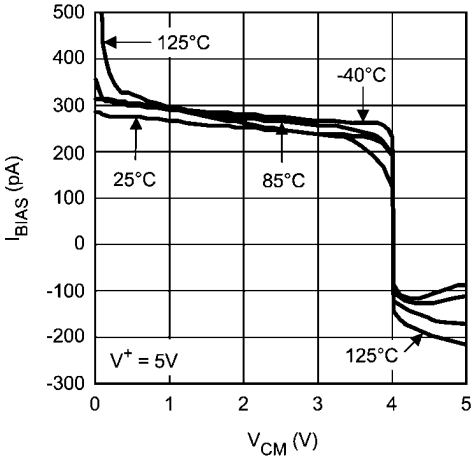
Input Bias Current vs. Common Mode Voltage



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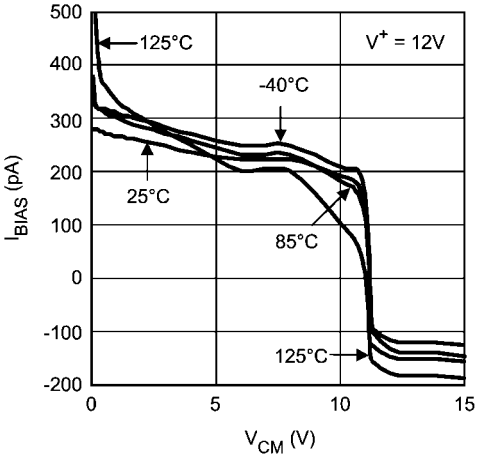
Input Bias Current vs. Common Mode Voltage



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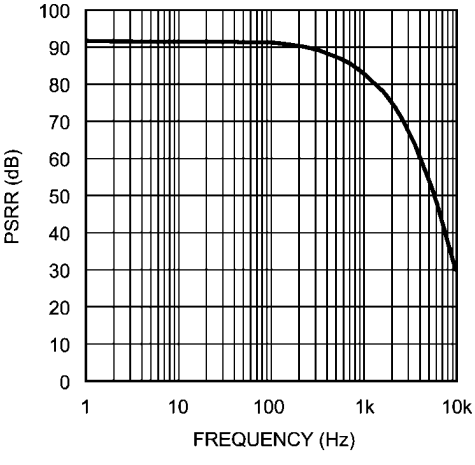
PSRR vs. Frequency



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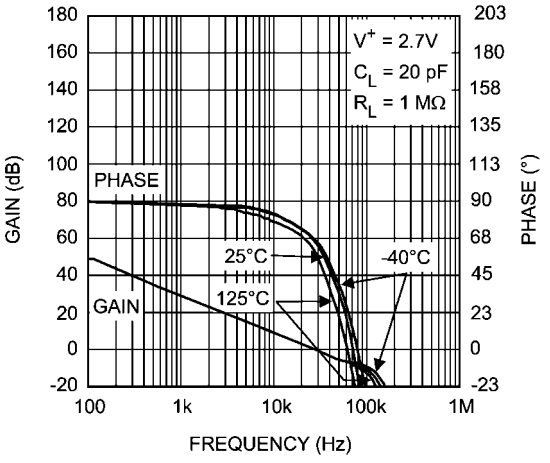
Frequency Response vs. Temperature



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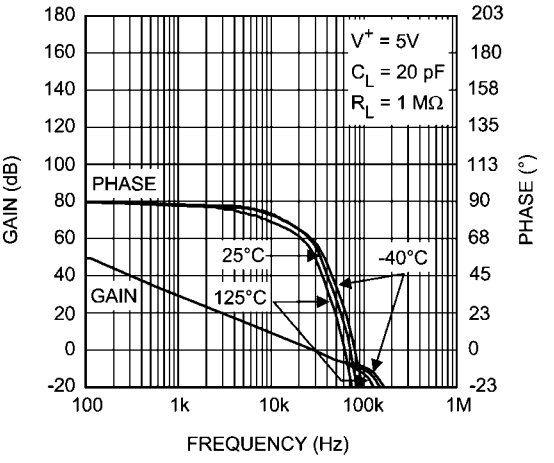
Frequency Response vs. Temperature



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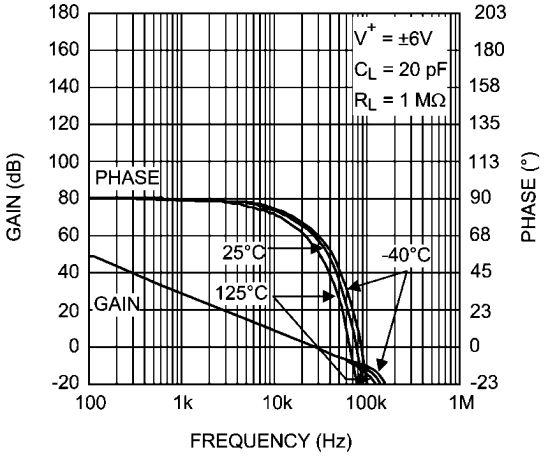
Frequency Response vs. Temperature



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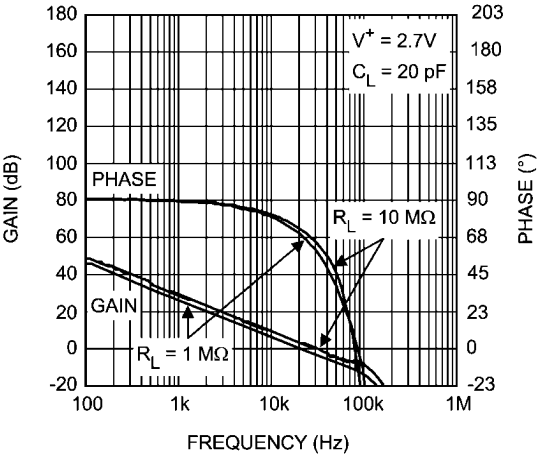
Frequency Response vs. R_L



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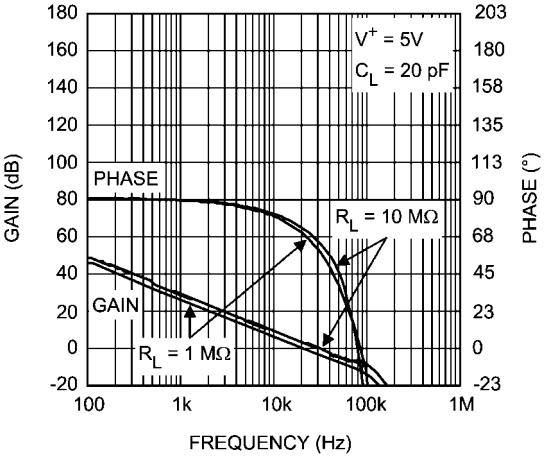
Frequency Response vs. R_L



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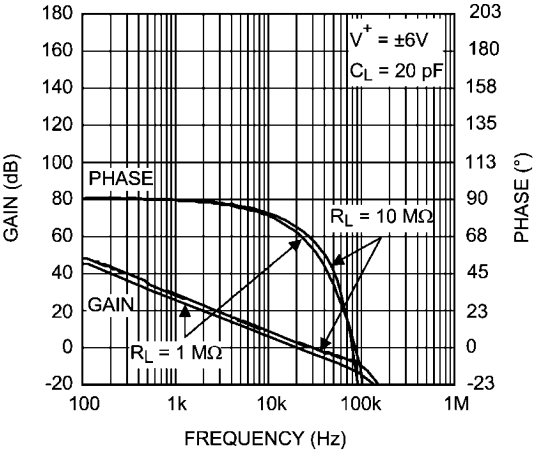
Frequency Response vs. R_L



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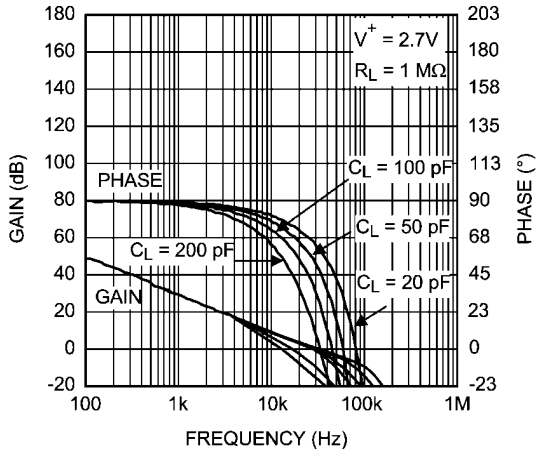
Frequency Response vs. C_L



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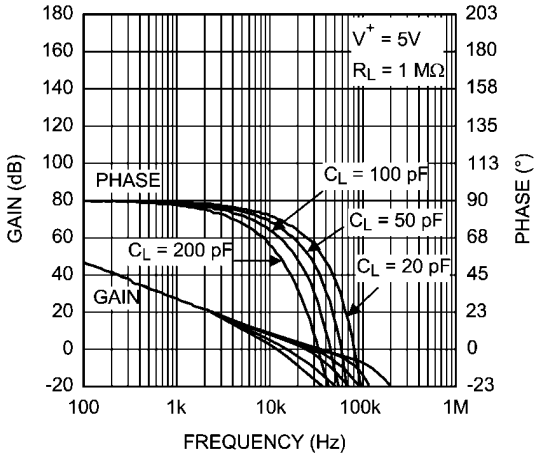
Frequency Response vs. C_L



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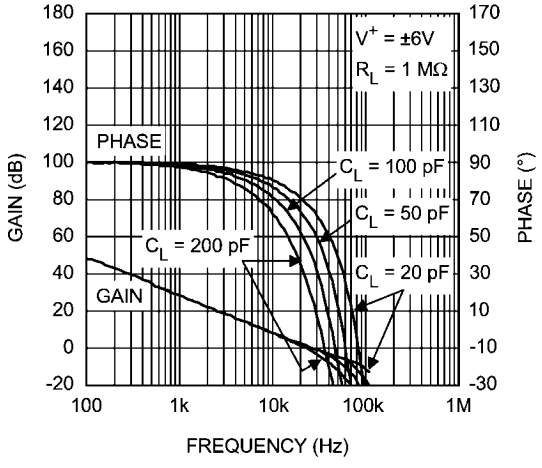
Frequency Response vs. C_L



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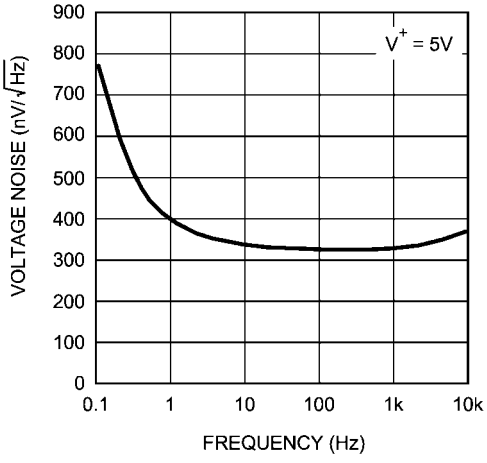
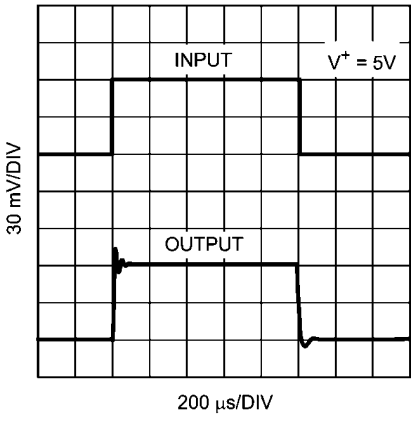
Voltage Noise vs. Frequency



20117026

Non-Inverting Small Signal Pulse Response



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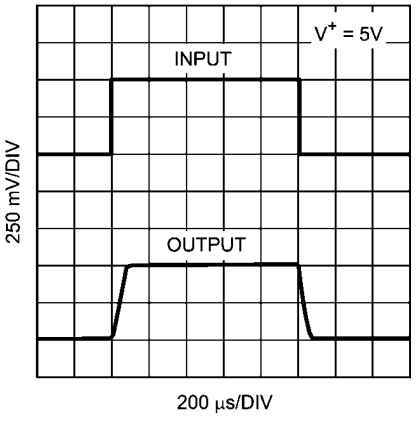
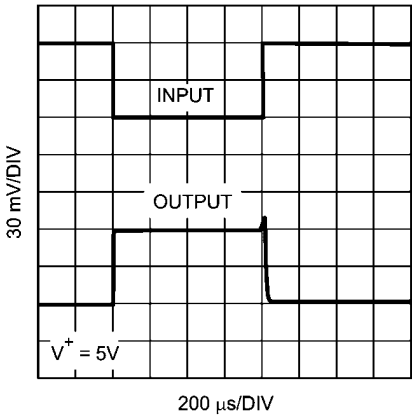
Non-Inverting Large Signal Pulse Response



20117030

Inverting Small Signal Pulse Response



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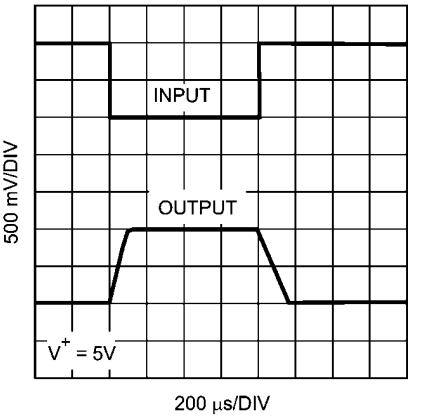
Inverting Large Signal Pulse Response



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Application Notes

The LPV511 is fabricated with National Semiconductor's state-of-the-art VIP50C process.

INPUT STAGE

The LPV511 has a rail-to-rail input which provides more flexibility for the system designer. As can be seen from the simplified schematic, rail-to-rail input is achieved by using in parallel, one PNP differential pair and one NPN differential pair. When the common mode input voltage (V_{CM}) is near V^+, the NPN pair is on and the PNP pair is off. When V_{CM} is near V^-, the NPN pair is off and the PNP pair is on. When V_{CM} is between V^+ and V^-, internal logic decides how much current each differential pair will get. This special logic ensures stable and low distortion amplifier operation within the entire common mode voltage range.

Because both input stages have their own offset voltage (V_{OS}) characteristic, the offset voltage of the LPV511 becomes a function of V_{CM}. V_{OS} has a crossover point at 1.0V below V^+. Refer to the 'V_{OS} vs. V_{CM}' curve in the Typical Performance Characteristics section. Caution should be taken in situations where the input signal amplitude is comparable to the V_{OS} value and/or the design requires high accuracy. In these situations, it is necessary for the input signal to avoid the crossover point.

The input bias current, I_B will change in value and polarity as the input crosses the transition region. In addition, parameters such as PSRR and CMRR which involve the input offset voltage will also be affected by changes in V_{CM} across the differential pair transition region.

Differential input voltage is the difference in voltage between the non-inverting (+) input and the inverting input (–) of the op amp. Due to the three series diodes across the two inputs, the absolute maximum differential input voltage is ±2.1V. This may not be a problem to most conventional op amp designs; however, designers should avoid using the LPV511 as a comparator.

OUTPUT STAGE

The LPV511 output voltage swing 100 mV from rails @ 3V supply, which provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.

The LPV511 Maximum Output Voltage Swing defines the maximum swing possible under a particular output load. The LPV511 output swings 110 mV from the rail @ 5V supply with an output load of 100 kΩ.

DRIVING CAPACITIVE LOAD

The LPV511 is internally compensated for stable unity gain operation, with a 27 kHz typical gain bandwidth. However, the unity gain follower is the most sensitive configuration to capacitive load. Direct capacitive loading reduces the phase margin of the op amp. When the output is required to drive a large capacitive load, greater than 100 pF, a small series resistor at the output of the amplifier improves the phase margin (see *Figure 1*).

In *Figure 1* , the isolation resistor R_{ISO} and the load capacitor C_L form a pole to increase stability by adding more phase margin to the overall system. The desired performance depends on the value of R_{ISO}. The bigger the R_{ISO} resistor value, the more stable V_{OUT} will be. But the DC accuracy is degraded when the R_{ISO} gets bigger. If there were a load resistor in *Figure 1*, the output voltage would be divided by R_{ISO} and the load resistor.

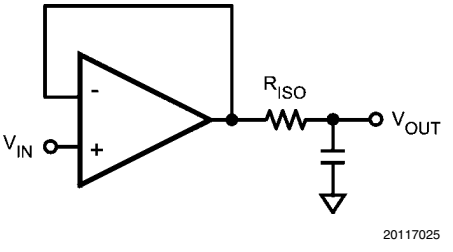

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FIGURE 1. Resistive Isolation of Capacitive Load

POWER SUPPLIES AND LAYOUT

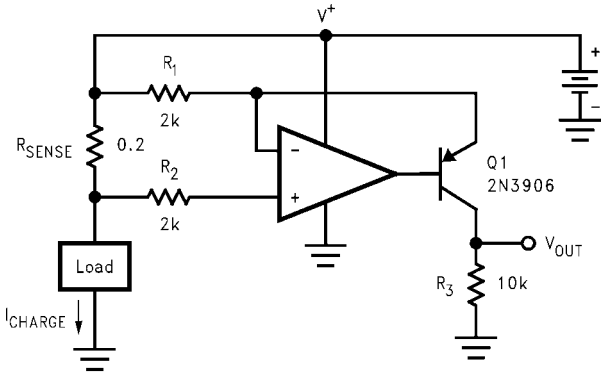
The LPV511 operates from a single 2.7V to 12V power supply. It is recommended to bypass the power supplies with a 0.1 µF ceramic capacitor placed close to the V^+ and V^- pins.

Ground layout improves performance by decreasing the amount of stray capacitance and noise at the op amp's inputs and outputs. To decrease stray capacitance, minimize PC board trace lengths and resistor leads, and place external components close to the op amps's pins.

Typical Applications

BATTERY CURRENT SENSING

The rail-to-rail common mode input range and the very low quiescent current make the LPV511 ideal to use in high side and low side battery current sensing applications. The high side current sensing circuit in *Figure 2* is commonly used in a battery charger to monitor the charging current in order to prevent over charging. A sense resistor R_{SENSE} is connected to the battery directly.



$$V_{OUT} = \frac{R_{SENSE} \bullet R_3}{R_1} \bullet I_{Charge} = 1\Omega \bullet I_{Charge}$$

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FIGURE 2. High Side Current Sensing

SUMMING AMPLIFIER

The LPV511 operational amplifier is a perfect fit in a summing amplifier circuit because of the rail-to-rail input and output and the sub-micro Amp quiescent current. In this configuration, the amplifier outputs the sum of the three input voltages.

The ratio of the sum and the output voltage is defined using feedback and input resistors.

$$V_{OUT} = R_F \left(\frac{V_{REF} - V_1}{R_1} + \frac{V_{REF} - V_2}{R_2} + \frac{V_{REF} - V_3}{R_3} \right) + V_{REF}$$

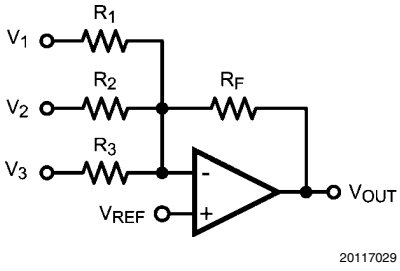

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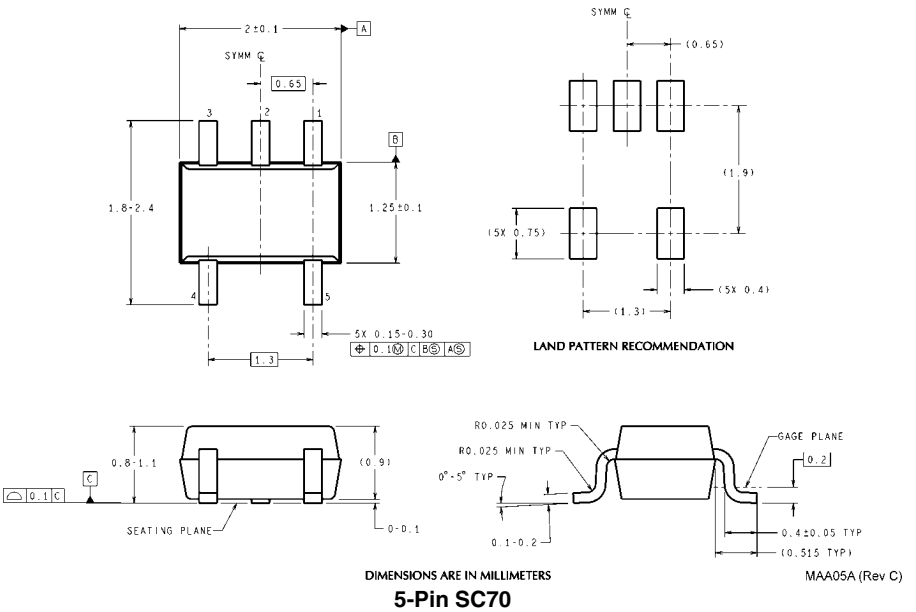
FIGURE 3. Summing Amplifier Circuit

Physical Dimensions inches (millimeters) unless otherwise noted



DIMENSIONS ARE IN MILLIMETERS

MAA05A (Rev C)

5-Pin SC70
NS Package Number MAA05A

Notes

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